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L5	L4 and ("channel length")	85	L5
L4	L3 and ("laser annealing")	99	L4
L3	((((257?$3)))!.CCLS.) and ("channel width")	1866	L3
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L8: Entry 1 of 1 File: USPT Nov 9, 1999

DOCUMENT-IDENTIFIER: US 5981974 A
TITLE: Semiconductor device and method for fabricating the same

Abstract Paragraph Left (1):
A semiconductor device includes a plurality of thin film transistors on a substrate having an insulating surface. A channel region of the thin film transistor comprises a crystalline Si film crystallized by a successive irradiation with a pulse laser beam in a scanning pitch P. A size Xs of the channel region in the scanning direction of the pulse laser beam and the scanning pitch P of the pulse laser beam have a relationship approximately equal to Xs=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (2):
The present invention relates to a semiconductor device comprising a plurality of thin film transistors formed on a substrate having an insulating surface, and a method for fabricating the same. More particularly, the present invention relates to a semiconductor device using thin film transistors having a crystalline Si film as an active region, and a method for fabricating the same.

Brief Summary Paragraph Right (4):
Recently, attempts have been made to form a high performance semiconductor element (for example, thin film transistor (TFT)) on an insulating substrate such as glass, or an insulating film for the development of a large-scale high-resolution liquid crystal display device, a low-cost monolithic-type liquid crystal display device comprising a driver circuit formed on the substrate where TFTs are formed, a high-speed, high-resolution adherent-type image sensor, a three-dimensional IC, and the like. Generally, a thin film silicon (Si) semiconductor is used for the semiconductor elements of these devices.

Brief Summary Paragraph Right (8):
In the above-described method (1), it is difficult to obtain a crystalline Si having a large grain size, since the crystallization proceeds simultaneously with the film formation. Thus, in this method, the thickness of the Si film must be increased in order to obtain a crystalline Si having a large grain size. However, since the increase of the film thickness only provides approximately the same crystal grain size as the film thickness, it is principally impossible to prepare a Si film having good crystallinity according to this method. Furthermore, since a high film formation temperature of 600.degree. C. or more is required for this method,

a cost problem arises in that it is impossible to use a less expensive glass substrate.

Brief Summary Paragraph Right (9):
The above-described method (2) requires a heating step at an elevated temperature of 600.degree. C. or more for several tens of hours in the crystallization step. Therefore, this method suffers lower productivity. Since this method utilizes a solid phase crystallization, the resulting crystal grains extend parallel to the surface of the substrate, and some of them even have a grain size of several .mu.m. However, because the grown crystal grains collide each other to form a grain boundary, the grain boundary acts as a trap level for carriers, and may be largely responsible for the reduction of the mobility of the TFT. Moreover, each crystal grain has a twin crystal structure which includes a large amount of crystal defects (which are called a twin crystal defect) even in a single crystal grain.

Brief Summary Paragraph Right (10):
For these reasons, the above-described method (3) is now mainly used for obtaining crystalline Si semiconductors. Since this method utilizes a fusion solidification method to conduct the crystallization, each crystal grain provides excellent crystallinity. Furthermore, because the selection of the wavelength of the light to be irradiated allows for only the efficient heating of the Si film to be annealed, it is possible to prevent the heat damaging of the glass substrate which is located below the Si film. Moreover, since this method does not require a long-term treatment as used in the method (2), it provides excellent productivity. Since a high power excimer laser annealing device has recently been developed for this method, this method would be applicable to large area substrates.

Brief Summary Paragraph Right (12):
The method described in Japanese Laid-open Patent Publication No. 8-201846 includes irradiating a driver monolithic-type active matrix substrate for a liquid crystal display apparatus with a pulse laser beam (hereinafter referred to as a laser pulse) in a manner that portions of the laser pulse are overlapped so as to crystallize the Si film corresponding to the active region of the element. The driver monolithic-type active matrix substrate refers to a substrate wherein pixel TFTs and a driver portion which drives the pixel TFTs are simultaneously formed on the same substrate. In addition, this method further includes irradiating the Si film forming the TFT constituting the driver portion with the edge portion of the laser pulse. Furthermore, alternative method is employed which includes irradiating the substrate with the laser pulse in a manner that the width of the semiconductor thin film with respect to the scanning direction of the laser pulse is more than or integral times as much as a pitch of the laser pulse.

Brief Summary Paragraph Right (13):
This method is the best among methods of crystallizing an Si film on an insulating substrate, but leaves a serious problem in the uniformity of the crystallinity. Specifically, a laser oscillator as a light source having an output power sufficient to irradiate a large area substrate has not yet been developed, and now the

surface of the substrate is irradiated by successively scanning a beam having an area of approximately 100-200 mm.sup.2. Therefore, as a matter of course, the non-uniformity of the crystallinity caused by the successive scanning of the laser has become a serious problem. Needless to say, the unevenness of the crystallinity directly relates to the characteristics of the semiconductor element, which causes the unevenness of the characteristics among the elements.

Brief Summary Paragraph Right (14):
The following illustrates the scanning and irradiation of the laser pulse in more detail. Generally, the scanning and irradiation with the laser pulse is conducted in a manner as illustrated in FIG. 14A. FIG. 14A is a schematic view showing the energy distribution (energy profile) of the laser beam viewed from the cross section in the scanning direction. In FIG. 14A, the symbols 608 and P denote a scanning direction and scanning pitch of the laser pulse, respectively. The energy distribution of each of the laser pulses 601-605 scanned in the scanning pitch P generally provides a Gaussian shape having a beam width 607. The Si film is successively irradiated with the laser pulses in the order of 601, 602, 603, 604 and 605.

Brief Summary Paragraph Right (17):
At the locations a, b, c and d in FIG. 14A, the laser pulse 602 is initially irradiated to crystallize an amorphous Si film so as to form a crystalline Si film. Thereafter, the laser pulses 603 and 604 are subsequently irradiated. At the time of irradiating the Si film with the original laser pulse 602, the energy supplied at each of the locations a, b, c and d is shown by the size of the arrow drawn in the vertical direction from each point. The energy is smallest at the location a, while it is largest at the location d. As a result, the crystallinity at the location a will be poorer than that at the location d. Similarly, the crystalinities at the locations b and c are poorer than that at the location d (that is, non-uniformity of the crystallinity occurs depending upon the locations). The laser pulses 603 and 604 are irradiated in order to repair this non-uniformity, however, as described above, these second and later laser pulses do not contribute to the crystallinity as the first laser pulse (602 in this case) does. Therefore, non-uniformity caused by the first laser pulse 602 is not completely repaired at each of the locations a, b, c and d.

Brief Summary Paragraph Right (18):
The crystallinity distribution of the crystalline Si film thus obtained in the laser scanning direction 608 has a serrated shape as shown by the symbol 609 in FIG. 14B. That is, a periodical non-uniformity is generated due to the laser scanning pitch P, and each of the locations a, b, c and d provides different crystallinity as shown in FIG. 14B. This non-uniformity of the crystallinity is mainly responsible for the non-uniformity of the characteristics of the crystalline Si film which is successively scanned and crystallized with the laser pulses. This causes the unevenness of the element characteristics, which results in display defects such as uneven display (contrast) in, for example, a liquid crystal display device.

Brief Summary Paragraph Right (19):
Japanese Laid-open Patent Publication No. 8-201846 focuses on the characteristic unevenness in the driver TFT of a driver monolithic-type active matrix substrate for a liquid crystal display device, and suggests a method of reducing the above-described unevenness. This patent publication describes a relationship between the width of the semiconductor thin film and the overlapping amount (i.e., the pitch) of the laser pulse at the time of the successive scanning, wherein the width of the semiconductor thin film is meant to be a width of a separated Si film forming an active region of the TFT (including both a source/drain region and a channel region). Since the TFT characteristics mainly depend on the film quality (crystallinity) of the channel region, it is difficult to accomplish an adequate uniformity intended for a plurality of the driver TFTs even by using the method as described in the above patent publication.

Brief Summary Paragraph Right (20):
According to Japanese Laid-open Patent Publication No. 7-92501, semiconductor elements (such as TFTs) are disposed on a straight line, and the straight line is irradiated with a laser light while controlling its position so as to crystallize the active region of the semiconductor element. In other words, the laser light is successively irradiated at the precisely controlled position so that the element regions disposed on each straight line are crystallized by a single irradiation with the laser light. Therefore, each TFT is irradiated with a single laser light so as not to create the overlapping portion at the time of the successive scanning. Each element is crystallized using each laser pulse alone and further using a relatively flat region around the peak top portion in its beam profile without creating an overlapping portion as illustrated in FIGS. 14A and 14B. Accordingly, the number of the laser pulses used for crystallizing all the elements on the substrate corresponds to the number of the element lines arranged on the straight lines.

Brief Summary Paragraph Right (23):
FIG. 15 is a schematic view depicted based on an interatomic force microscope (AFM) image of the surface condition of a crystalline silicon film which is actually crystallized by the strong light irradiation. The full scale in the X-Y direction in FIG. 15 is 2.0 .mu.m, and the full scale in the Z direction is 50 nm. When a capacity component is fabricated using a crystalline silicon film as one of the electrodes, the capacity will be higher than the designed value due to its surface roughness. When its crystallinity is varied by the laser scanning as described with reference to FIGS. 14A and 14B, the resulting silicon film has an increased surface roughness which results in a larger variation of the capacity values. The capacity variation of a storage capacitor connected to the pixel TFT in a liquid crystal display device may cause an uneven display such as flicker of the screen.

Brief Summary Paragraph Right (25):
The semiconductor device of this invention includes a plurality of thin film transistors on a substrate having an insulating surface. A channel region of said thin film transistor comprises a crystalline Si film crystallized by a successive irradiation with a

pulse laser beam in a scanning pitch P, and a size Xs of said channel region in the scanning direction of said pulse laser beam and said scanning pitch P of said pulse laser beam have a relationship approximately equal to Xs=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (26):
In one embodiment of the invention, said substrate is an active matrix substrate having the corresponding number of pixel electrodes to that of said thin film transistors, and said thin film transistors are those for switching the pixel connected to said pixel electrodes.

Brief Summary Paragraph Right (27):
In another embodiment of the invention, said substrate is a driver monolithic-type active matrix substrate having an active matrix portion and a driver circuit, and said thin film transistors constitute a switch for said active matrix portion and said driver circuit.

Brief Summary Paragraph Right (30):
According to another aspect of the invention, a method for fabricating a semiconductor device is provided. The method includes the steps of: forming a Si film on a substrate having an insulating surface; crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P; and patterning said crystallized Si film so as to form a plurality of thin film transistor element regions, wherein the scanning direction of said pulse laser beam is vertical to the channel direction of said thin film transistor, and the channel width X.sub.W of said thin film transistor and the scanning pitch P of said pulse laser beam have a relationship approximately equal to X.sub.W =nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (31):
According to still another aspect of the invention, the method includes the steps of: forming a Si film on a substrate having an insulating surface; crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P; and patterning said crystallized Si film so as to form a plurality of thin film transistor element regions, wherein the scanning direction of said pulse laser beam is parallel to the channel direction of said thin film transistor, and the channel length X.sub.L of said thin film transistor and the scanning pitch P of said pulse laser beam have a relationship approximately equal to X.sub.L =nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (32):
According to still another aspect of the invention, the method includes the steps of: forming a Si film on a substrate having an insulating surface; patterning said Si film so as to form a plurality of thin film transistor element regions, wherein the subsequent scanning direction of said pulse laser beam is vertical to the channel direction of said thin film transistor, and the channel width of said thin film transistor is X.sub.W ; and crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P that provides a

relationship approximately equal to X.sub.W =nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (33):
According to still another aspect of the invention, the method includes the steps of: forming a Si film on a substrate having an insulating surface; patterning said Si film so as to form a plurality of thin film transistor element regions, wherein the subsequent scanning direction of said pulse laser beam is parallel to the channel direction of said thin film transistor, and the channel length of said thin film transistor is X.sub.L ; and crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P that provides a relationship approximately equal to X.sub.L =nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (34):
In one embodiment of the invention, the method further includes the step of heating said Si film formed on said substrate before the irradiation with said pulse laser beam, so as to crystallize said Si film in a solid phase.

Brief Summary Paragraph Right (39):
In still another embodiment of the invention, the beam shape of said pulse laser beam is a slender rectangle on the irradiated surface, and said pulse laser beam is successively irradiated in a direction vertical to the longer side of said rectangle beam.

Brief Summary Paragraph Right (40):
According to still another aspect of the invention, the semiconductor device includes a plurality of thin film transistors on a substrate having an insulating surface. The channel region of said thin film transistor comprises a crystalline Si film crystallized by a successive irradiation with a pulse laser beam in a scanning pitch P, and an arrangement interval Xp of said channel region in the scanning direction of said pulse laser beam and a scanning pitch P of said pulse laser beam have a relationship approximately equal to Xp=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (41):
According to still another aspect of the invention, the semiconductor device includes a plurality of thin film transistors driving a pixel electrode and a storage capacitor connected parallel to the pixel capacitor of said thin film transistor on a substrate having an insulating surface. The channel region of said thin film transistor, and one of electrodes of said storage capacitor comprise a crystalline Si film crystallized by a successive irradiation with a pulse laser beam, and an arrangement interval Xp of said channel region in the scanning direction of said pulse laser beam and an arrangement interval of said electrode of said storage capacitor are approximately the same, and said interval Xp and the scanning pitch P of said pulse laser beam have a relationship approximately equal to Xp=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (42):
According to still another aspect of the invention, the

semiconductor device comprising a plurality of thin film transistors driving pixel electrodes, and a plurality of thin film transistors which constitute a driver circuit driving said thin film transistors driving pixel electrodes. The channel regions of said thin film transistors driving said pixel electrodes and said thin film transistors which constitute said driver circuit comprise a crystalline Si film crystallized by a successive irradiation with a pulse laser beam, and an arrangement interval Xp of said channel region in the scanning direction of said pulse laser beam and the scanning pitch P of said pulse laser beam have a relationship approximately equal to Xp=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (47):
According to still another aspect of the invention, a method for fabricating a semiconductor device is provided. The method includes the steps of: forming a Si film on a substrate having an insulating surface; crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P; and patterning said crystallized Si film so as to form a plurality of thin film transistor element regions, wherein an arrangement interval Xp of said thin film transistor in the scanning direction of said pulse laser beam and the scanning pitch P of said pulse laser beam have a relationship approximately equal to Xp=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (48):
According to still another aspect of the invention, the method includes the steps of: forming a Si film on a substrate having an insulating surface; patterning said Si film so as to form a plurality of thin film transistor element regions, wherein an arrangement interval of the channel region of said thin film transistors in the subsequent scanning direction of a laser beam is Xp; and crystallizing said Si film by successively irradiating said Si film with a pulse laser beam in a scanning pitch P that provides a relationship approximately equal to Xp=nP where n is an integer of 1 or more.

Brief Summary Paragraph Right (49):
In one embodiment of the invention, the method further includes the step of heating said Si film formed on said substrate before the irradiation with said pulse laser beam, so as to crystallize said Si film in a solid phase.

Brief Summary Paragraph Right (54):
In still another embodiment of the invention, the beam shape of said pulse laser beam is a slender rectangle on the irradiated surface, and said pulse laser beam is successively irradiated in a direction vertical to the longer side of said rectangle beam.

Drawing Description Paragraph Right (1):
FIG. 1 is a schematic plan view of an active matrix substrate according to a preferred embodiment of the present invention.

Drawing Description Paragraph Right (2):
FIGS. 2A to 2E are schematic views for illustrating a method for fabricating the active matrix substrate of FIG. 1, which are sectional views taken along the line II--II of FIG. 1.

Drawing Description Paragraph Right (3):
FIG. 3 is a schematic plan view of a semiconductor device comprising a plurality of CMOS circuits formed on a substrate according to another preferred embodiment of the present invention.

Drawing Description Paragraph Right (6):
FIG. 6 is a schematic plan view of an active matrix substrate according to still another preferred embodiment of the present invention.

Drawing Description Paragraph Right (7):
FIGS. 7A to 7E are schematic sectional views for illustrating a method for fabricating the active matrix substrate of FIG. 6.

Drawing Description Paragraph Right (8):
FIG. 8 is a schematic plan view of an active matrix substrate comprising a storage capacitor according to still another preferred embodiment of the present invention.

Drawing Description Paragraph Right (9):
FIGS. 9A to 9E are schematic sectional views for illustrating a method for fabricating the active matrix substrate of FIG. 8.

Drawing Description Paragraph Right (10):
FIG. 10 is a schematic plan view of a driver monolithic-type active matrix substrate according to still another preferred embodiment of the present invention.

Drawing Description Paragraph Right (11):
FIG. 11 is a schematic plan view for illustrating a method for fabricating a CMOS circuit which constitutes the driver circuit of the active matrix substrate of FIG. 10.

Drawing Description Paragraph Right (13):
FIGS. 13A to 13F are schematic sectional views for illustrating a method for fabricating the pixel TFT of the active matrix substrate of FIG. 10.

Drawing Description Paragraph Right (14):
FIG. 14A is a schematic view for illustrating the energy distribution of the laser beam viewed from the cross section in the scanning direction of a laser pulse.

Detailed Description Paragraph Right (1):
In the present specification, the term "a size of the channel region of a TFT in the scanning direction of a laser pulse" is meant to include a length of the channel region of the TFT in the scanning direction of a laser pulse. For example, when the scanning direction of a laser pulse is parallel to the channel direction of a TFT, a size of the channel region is a length of the channel (a length of the TFT in the channel direction), and when the scanning direction of a laser pulse is vertical to the channel direction of a TFT, a size of the channel region is a width of the channel (a length of the TFT in the direction vertical to the channel direction).

Detailed Description Paragraph Right (2):
The term "an arrangement interval of the channel region of a TFT in the scanning direction of a laser pulse" is meant to include an interval between the TFTs placed on the lines adjacent to each other in the scanning direction of a laser pulse.

Detailed Description Paragraph Right (4):
A preferred embodiment of the present invention is illustrated with reference to FIG. 1 and FIGS. 2A to 2E. The present embodiment is a case where the present invention is applied to an active matrix substrate for a liquid crystal display device. FIG. 1 is a schematic plan view of this active matrix substrate. FIGS. 2A to 2E are schematic views for illustrating a method for fabricating the active matrix substrate of FIG. 1, which are sectional views taken along the line II--II of FIG. 1.

Detailed Description Paragraph Right (5):
As shown in FIG. 1, N-type TFTs 121 are formed in a matrix shape as an element for switching each pixel on the active matrix substrate (several hundred thousand TFTs 121 are arranged on an actual active matrix substrate).

Detailed Description Paragraph Right (6):
The structure of the active matrix substrate is illustrated together with a method for fabricating it with reference to FIGS. 2A to 2E. First, as shown in FIG. 2A, a base film 102 comprising SiO.sub.2 and having a thickness of approximately 300 nm is formed on a glass substrate 101 by, for example, a sputtering method. The SiO.sub.2 film 102 is provided so as to prevent the impurities contained in the glass substrate 101 from diffusing.

Detailed Description Paragraph Right (8):
Then, as shown in FIG. 2B, an undesired portion of the a-Si film 103 is removed by any suitable method so as to form an island-like Si film 108 constituting an active region of a TFT (a source/drain region and a channel region). When the glass substrate 101 is viewed from the top, the active region 108 of each TFT 121 is disposed as shown in FIG. 1, wherein the symbol 114 of FIG. 1 represents a source region of the resulting TFT 121, 115 represents a drain region, 127 represents a channel region, and 128 represents an offset region. A carrier moves from the source region 114 to the drain region 115 at the time of driving the TFT 121. In other words, the channel direction, which is a carrier moving direction, is a direction from the top to the bottom of the paper in FIG. 1.

Detailed Description Paragraph Right (9):
Thereafter, as shown in FIG. 2C, the island-like a-Si film 108 is irradiated with a laser pulse 107 to be crystallized. The laser beams that can be used include XeCl excimer laser (having a wavelength of 308 nm and a pulse width of 40 nsec). The laser pulse 107 is irradiated at an energy density of about 200 to 350 mJ/cm.sup.2, for example about 300 mJ/cm.sup.2, while heating the glass substrate 101 to about 200 to 500.degree. C., for example about 400.degree. C. at the time of the irradiation.

Detailed Description Paragraph Right (10):

The laser pulse 107 is shaped with a homogenizer so that the beam on the substrate surface has a slender rectangle shape (e.g., 300 mm.times.0.2 mm), and is successively scanned in the direction vertical to its longer side. In the present embodiment, the scanning direction of the laser pulse 107 with respect to the TFT 121 is shown by the arrow 124 in FIG. 1. That is, the scanning direction 124 of the laser pulse 107 is parallel to (in the same direction as) the channel direction of the TFT 121. In the present embodiment, the overlapping amount of the laser pulse 107 in the successive scanning is set to be 95%. Therefore, the scanning pitch P in FIG. 1 is 10 .mu.m, and any one point of the a-Si film 108 is subjected to the laser irradiation twenty times each.

Detailed Description Paragraph Right (11):
According to this step, the a-Si film 108 is heated to a temperature higher than its melting point, and fused and solidified to form a crystalline Si film 108a having good crystallinity. The crystallinity distribution of the crystalline Si film 108a has a serrated shape as shown by the symbol 126 of FIG. 1, wherein the horizontal axis indicates the crystallinity and a further right-hand direction provides better crystallinity. The mechanism that the crystallinity distribution has a serrated shape is as illustrated above with reference to FIG. 14B, and therefore is not mentioned here.

Detailed Description Paragraph Right (12):
Then, as shown in FIG. 2D, a SiO.sub.2 film having a thickness of about 20 to 150 nm, about 100 nm in this embodiment is formed as a gate insulating film 109 so that it covers the above-described crystalline Si film 108a which constitutes an active region. In the present embodiment, the SiO.sub.2 film is formed by using TEOS (tetraethoxy orthosilicate) as a starting material, and decomposing and depositing it together with oxygen at a substrate temperature of about 150 to 600.degree. C., preferably about 300 to 450.degree. C., by an RF plasma CVD method. Alternatively, it is possible to form the SiO.sub.2 film by using TEOS as a starting material together with ozone gas at a substrate temperature of about 350 to 600.degree. C., preferably about 400 to 550.degree. C., by a reduced pressure CVD method or an ordinary pressure CVD method.

Detailed Description Paragraph Right (14):
The anodic oxidation is conducted by, for example, initially increasing the voltage to 220 V at a constant current in an ethylene glycol solution containing about 1 to 5% tartaric acid, and then maintaining this condition for 1 hour. In the present embodiment, the resulting anodically oxidized layer 111 has a thickness of about 200 nm. An offset gate region is formed from the anodically oxidized layer 111 in the subsequent ion doping step. Therefore, the offset gate region having the prescribed length is obtained by forming the anodically oxidized layer having the prescribed thickness. The offset gate region is provided for the purpose of reducing the leak current when the TFT is not operated. Moreover, the channel length X.sub.L of the TFT 121 is determined by the gate width of the resulting gate electrode 110.

Detailed Description Paragraph Right (17):
Moreover, as shown in FIG. 2E, a SiO.sub.2 film having a thickness

of approximately 600 nm is formed as an interlayer insulating film 116. The SiO.sub.2 film is formed using TEOS as a starting material by a plasma CVD method together with oxygen, or by a reduced pressure CVD electrode is patterned so that the resulting gate width is 10 .mu.m. That is, both the channel length X.sub.L of the channel region 127 of the TFT 121 as shown in FIG. 1 and the scanning pitch P of the laser pulse are set to be 10 .mu.m. The crystallinity distribution of the channel region 127 of the TFT 121 is represented by the shape 131a, 131b and 131c for each TFT present in different lines, all of which have the same shape (i.e., the same crystallinity distribution). Therefore, each TFT has the same crystallinity distribution. In other words, since all the crystallinity distributions resulted from the scanning of the laser pulse are similarly included in the channel region 127 of the TFT 121, there is no unevenness in the crystallinity among the TFTs 121.

Detailed Description Paragraph Right (21):
Each TFT 121 which is actually fabricated according to the above-described steps provides excellent characteristics having a field-effect mobility of 60 to 80 cm.sup.2 /Vs, and a threshold voltage of 1.5 to 2 V in all the panels fabricated. Moreover, the TFTs 121 in the panel have excellent uniformity and a field-effect mobility difference of approximately .+-.8%, and a threshold voltage difference of approximately .+-.0.2 V. When a liquid crystal display device is fabricated using the active matrix substrate of the present embodiment and the overall display is performed, the uneven display due to the non-uniformity of the TFT characteristics is largely reduced and a liquid crystal display device having higher display quality is obtained.

Detailed Description Paragraph Right (22):
Another preferred embodiment of the present invention is illustrated with reference to FIG. 3, FIG. 4 and FIGS. 5A to 5F. The present embodiment is a case where the present invention is applied to a semiconductor device comprising a plurality of CMOS circuits (circuit elements) formed on a substrate. The CMOS circuit (circuit element) is composed complementarily of an N-type TFT and a P-type TFT and constitutes a basis for a thin film integrated circuit.

Detailed Description Paragraph Right (24):
As shown in FIG. 3, the CMOS circuit comprises a plurality of N-type TFTs 222 and P-type TFTs 223 formed on a substrate, and FIG. 5F shows its finished sectional structure. The following illustrates the structure of the semiconductor device together with a method for fabricating the device.

Detailed Description Paragraph Right (25):
First, as shown in FIG. 5A, a base film 202 comprising SiO.sub.2 and having a thickness of approximately 300 nm is formed on a glass substrate 201 by, for example, a sputtering method. The base film 202 is provided so as to prevent the impurities contained in the glass substrate 201 from diffusing. Then, an intrinsic (I-type) amorphous Si (a-Si) film 203 having a thickness of about 20 to 100 nm, for example about 50 nm, is formed by a reduced pressure CVD method, a plasma CVD method, or the like.

Detailed Description Paragraph Right (26):
Then, a photosensitive resin (e.g., photoresist) is applied onto the a-Si film 203, exposed to light, and developed so as to form a photoresist mask 204. The a-Si film 203 is exposed in a slit shape in the region 200 by the throughhole of the photoresist mask 204 as shown in FIG. 4. When the substrate of FIG. 5A is viewed from the top, the a-Si film 203 is exposed in the region 200 as shown in FIG. 4, and the other portions are masked by the photoresist.

Detailed Description Paragraph Right (27):
Then, as shown in FIG. 5A, Ni is deposited on a glass substrate 201 on which the base film 202, the a-Si film 203 and the mask 204 are formed, so as to form a thin film 205. In the present embodiment, the thickness of the Ni thin film 205 is adjusted to approximately 1 nm or less by making the distance between the deposition source and the glass substrate 201 greater than usual to reduce the deposition rate. The surface density of the Ni thin film 205 which is actually measured is approximately 1.times.10.sup.13 atom s /cm.sup.2.

Detailed Description Paragraph Right (29):
As shown in FIG. 5B, this crystallization of the a-Si film 203 proceeds in the direction vertical to the glass substrate 201 using as a nucleus Ni which is added to the surface of the a-Si film 203 in the region 200, so as to form a crystalline Si-film 203b (see also FIG. 4). Then, the crystal is grown in the horizontal direction (the direction parallel to the glass substrate 201) from the region 200 to a region surrounding the region 200 as indicated by the arrow 206 in FIGS. 4 and 5B, so as to form a horizontally grown crystalline Si film 203c. The other regions in the a-Si film 203 remain as an amorphous Si region 203d. The size of the grown crystal in the direction parallel to the glass substrate 201 which is actually measured is approximately 40 .mu.m.

Detailed Description Paragraph Right (30):
Thereafter, as shown in FIG. 5C, the Si film 203 is irradiated with a laser pulse 207 to be recrystallized. The laser beams that can be used include XeCl excimer laser (having a wavelength of 308 nm and a pulse width of 40 nsec). The laser pulse 207 irradiates at an energy density of about 200 to 350 mJ/cm.sup.2, for example about 320 mJ/cm.sup.2, while heating the glass substrate 201 to about 200 to 500.degree. C., for example about 400.degree. C. at the time of the irradiation. The laser pulse 207 is shaped with a homogenizer so that the beam on the substrate surface has a slender rectangle shape (e.g., 150 mm.times.1 mm), and is successively scanned in the direction vertical to its longer side. The laser scanning direction with respect to the final TFT element arrangement have a relationship as illustrated in FIG. 3, and its scanning direction is indicated by the symbol 224. In the present embodiment, the overlapping amount of the beam in the successive scanning is set to be 90%. Therefore, the scanning pitch P in FIG. 3 is 100 .mu.m, and any one point of the a-Si film 203 is subjected to the laser irradiation ten times each.

Detailed Description Paragraph Right (31):
According to this step, the crystalline Si film regions 203b and

203c are heated to a temperature higher than their melting points, and fused and solidified to be recrystallized using a portion thereof as a seed crystal and to form Si film regions 203b' and 203c' having better crystallinity. The a-Si film region 203d is crystallized to form a crystalline Si-film 203a. The crystallinity distribution of the crystalline Si film 203a has a serrated shape as shown by the symbol 226 of FIG. 3, wherein the horizontal axis indicates the crystallinity and a further right-hand direction provides better crystallinity.

Detailed Description Paragraph Right (32):
Thereafter, the prescribed portion of crystalline Si film is removed by etching so as to be separated so that a high quality crystalline Si film region 203c' constitutes active regions (element regions) 208n and 208p of the TFT, as shown in FIGS. 4 and 5D. When the glass substrate 201 is viewed from the top, an active region 208 (208n, 208p) for each of the TFTs 222 and 223 is disposed as shown in FIG. 4, respectively. In FIG. 3, the regions 214 (214n, 214p)/215 (215n, 215p) constitute a source/drain region. The region 213 (227), specifically 213n, 213p (227n, 227p) constitutes a channel region.

Detailed Description Paragraph Right (33):
As can be seen from FIG. 3, the scanning direction 224 of the laser pulse is designed to be vertical to the channel direction of the TFT (i.e., the moving direction of the carrier, corresponding to the direction from the left to the right in the paper) in the present embodiment. Therefore, the channel size of the TFT 222 in the laser scanning direction 224 is a channel width X.sub.W, and the active region 208 is formed so that the channel width X.sub.W is the same as the laser scanning pitch P (100 .mu.m). The crystallinity distribution of the channel region 227 of the TFT 121 is represented by the shape 231a, 231b and 231c for each TFT in different lines, all of which have the same area (i.e., having the same crystallinity). Therefore, although each TFT in different lines has a different crystallinity distribution, each TFT has the same crystallinity. In other words, since all the crystallinity distributions resulting from the scanning of the laser pulse are included in the channel region 227 of each TFT in the same amount, there is no unevenness in the crystallinity among the TFTs.

Detailed Description Paragraph Right (34):
Then, as shown in FIG. 5E, a SiO.sub.2 film having a thickness of about 100 nm is formed as a gate insulating film 209 so as to cover the crystalline Si films 208n and 208p which constitute an active region. In the present embodiment, the gate insulating film 209 is formed by using TEOS as a starting material, and decomposing and depositing it together with oxygen at a substrate temperature of about 300 to 400.degree. C. by an RF plasma CVD method. Preferably, after forming the film, the gate insulating film 209 is annealed at about 400 to 600.degree. C. for several hours under an inert gas atmosphere in order to improve a bulk property of the gate insulating film 209 as well as the interface property between the crystalline Si film and the gate insulating film 209.

Detailed Description Paragraph Right (37):
As a result, N-type impurity regions 214n and 215n, and P-type

impurity regions 214p and 215p are formed, which can result in the formation of an N-channel type TFT 222 and a P-channel type TFT 223, as shown in FIGS. 5E and 5F. When the substrate is viewed from the top, as shown in FIG. 4, the crystal growth direction 206 in the active regions 208n and 208p is parallel to the carrier moving direction (i.e., from the source to the drain direction). This arrangement provides a TFT having higher mobility.

Detailed Description Paragraph Right (41):
Still another preferred embodiment of the present invention is illustrated with reference to FIGS. 6 and FIGS. 7A to 7E. The present embodiment is a case where the present invention is applied to an active matrix substrate for a liquid crystal display device. FIG. 6 is a schematic plan view of the active matrix substrate. FIGS. 7A to 7E are schematic sectional views for illustrating a method for fabricating the active matrix substrate of FIG. 6.

Detailed Description Paragraph Right (42):
As shown in FIG. 6, the active matrix substrate comprises an N-type TFT 321 formed in a matrix shape as an element for switching each pixel electrode. FIG. 7E is a schematic sectional view of the finished active matrix substrate.

Detailed Description Paragraph Right (43):
The structure of the active matrix substrate is illustrated together with a method for fabricating it with reference to FIGS. 7A to 7E. First, as shown in FIG. 7A, a base film 302 comprising SiO.sub.2 and having a thickness of approximately 300 nm is formed on a glass substrate 301 by, for example, a sputtering method. The SiO.sub.2 film 302 is provided so as to prevent the impurities contained in the glass substrate 301 from diffusing.

Detailed Description Paragraph Right (45):
Thereafter, as shown in FIG. 7B, the a-Si film 303 is irradiated with a laser pulse 307 to be crystallized. The laser beams that can be used include XeCl excimer laser (having a wavelength of 308 nm and a pulse width of 40 nsec). The laser pulse 307 irradiates at an energy density of about 200 to 350 mJ/cm.sup.2, for example about 300 mJ/cm.sup.2, while heating the glass substrate to about 200 to 500.degree. C., for example about 400.degree. C., at the time of the irradiation. The laser pulse 307 is shaped with a homogenizer so that the beam on the substrate surface has a slender rectangle shape (e.g., 150 mm.times.1 mm), and is successively scanned in the direction vertical to its longer side, i.e., the laser scanning direction 324 in FIG. 6. In the present embodiment, the overlapping amount of the laser pulse 307 in the successive scanning is set to be 95%. Therefore, the scanning pitch P in FIG. 6 is 50 .mu.m, and any one point of the a-Si film 303 is subjected to the laser irradiation twenty times each. According to this step, the a-Si film 303 is heated to a temperature higher than its melting point, and fused and solidified to form a crystalline Si film 303a having good crystallinity.

Detailed Description Paragraph Right (46):
Then, as shown in FIG. 7C, an undesired portion of the a-Si film 303a is removed by any suitable method so as to form an island-like Si film 308a constituting an active region (a source region, a

drain region and a channel region) of TFT. When the substrate 301 is viewed from the top, the island-like crystalline Si film 308a which constitutes an active region of each TFT is disposed as shown in FIG. 6. The arrangement interval X.sub.p of the island-like crystalline Si film 308a in the laser scanning direction 324 is designed to be 100 .mu.m. Thus, the arrangement interval X.sub.p of the TFT is twice as much as the laser scanning pitch P.

Detailed Description Paragraph Right (48):
Then, as shown in FIG. 7D, a SiO.sub.2 film having a thickness of about 20 to 150 nm (about 100 nm in the present embodiment) is formed as a gate insulating film 309 so as to cover the island-like crystalline Si film 308a which constitutes an active region. In the present embodiment, the SiO.sub.2 film is formed by using TEOS (tetraethoxy orthosilicate) as a starting material, and depositing and accumulating it together with oxygen at a substrate temperature of about 150 to 600.degree. C., preferably about 300 to 450.degree. C. by an RF plasma CVD method. Alternatively, it is possible to form the SiO.sub.2 film by using TEOS as a starting material together with ozone gas at a substrate temperature of about 350 to 600.degree. C., preferably about 400 to 550.degree. C., by a reduced pressure CVD method or an ordinary pressure CVD method.

Detailed Description Paragraph Right (56):
Each TFT 321 which is actually fabricated according to the above-described steps provides excellent characteristics having a field-effect mobility of 40 to 80 cm.sup.2 /Vs, and a threshold voltage of 1.5 to 3 V in all the fabricated panels. Moreover, the TFTs 321 in the panel have excellent uniformity and a field-effect mobility difference of approximately .+-.8%, and a threshold voltage difference of approximately .+-.0.2 V, although there is some variation in the TFT characteristics among different panels within the above-described ranges. When a liquid crystal display device is fabricated using the active matrix substrate of the present embodiment and the overall display is performed, the uneven display due to the non-uniformity in the TFT characteristics is largely reduced and a liquid crystal display device having higher display quality is obtained.

Detailed Description Paragraph Right (57):
Still another preferred embodiment of the present invention is illustrated with reference to FIG. 8 and FIGS. 9A to 9E. The present embodiment is also a case where the present invention is applied to an active matrix substrate for a liquid crystal display device. This active matrix substrate further comprises a storage capacitor Cs parallel to the pixel liquid crystal capacitor in the drain region side of the TFT. FIG. 8 is a schematic plan view of the active matrix substrate. FIGS. 9A to 9E are schematic views for illustrating a method for fabricating the active matrix substrate of FIG. 8.

Detailed Description Paragraph Right (58):
As shown in FIG. 8, the active matrix substrate comprises an N-type TFT 421 formed in a matrix shape as an element for switching each pixel electrode, and a storage capacitor 434 in the drain side of the TFT. FIG. 9E is a schematic sectional view of the finished active matrix substrate.

Detailed Description Paragraph Right (59):
The structure of the active matrix substrate is illustrated together with a method for fabricating it with reference to FIGS. 9A to 9E. First, as shown in FIG. 9A, a base film 402 comprising SiO.sub.2 and having a thickness of approximately 300 nm is formed on a glass substrate 401 by, for example, a sputtering method. The SiO.sub.2 film 402 is provided so as to prevent the impurities of the glass substrate 401 from diffusing.

Detailed Description Paragraph Right (63):
When the substrate is viewed from the top, it is as shown in FIG. 8. That is, each TFT 421 and the storage capacitor Cs 434 are disposed on the same line at an equal interval (i.e., the laser scanning pitch P) in the scanning direction 424 of the subsequent laser irradiation. In the present embodiment, the arrangement interval Xp of the TFT is set to be 100 .mu.m.

Detailed Description Paragraph Right (65):
Then, as shown in FIG. 9C, a laser pulse 407 irradiates to crystallize the island-like a-Si film 408. The laser beams that can be used include an XeCl excimer laser (having a wavelength of 308 nm and a pulse width of 40 nsec). The laser pulse 407 irradiates at an energy density of about 200 to 350 mJ/cm.sup.2, for example about 300 mJ/cm.sup.2, while heating the substrate to about 200 to 500.degree. C., for example about 400.degree. C. at the time of the irradiation. The laser pulse 407 is successively scanned in the direction 424 as shown in FIG. 8. The laser pulse 407 is shaped with a homogenizer so that the beam on the substrate surface has a slender rectangle shape (e.g., 150 mm.times.1 mm), and its short side direction is the scanning direction. Because the overlapping amount of the laser beam is set to be 90%, the laser scanning pitch P is 100 .mu.m, and any one point of the a-Si film 403 is subjected to the laser irradiation ten times each. Since the arrangement interval Xp of the island-like a-Si film 408 comprising the TFT active region and the storage capacitor Cs in the laser scanning direction 424 is set to be 100 .mu.m, it is the same as the laser scanning pitch P. According to this step, the a-Si film 403 is heated to a temperature higher than its melting point, and fused and solidified so as to form a crystalline Si film 403a having good crystallinity, and so as to activate the impurity in the continuous region 415 including the drain region and the lower electrode of the storage capacitor Cs and reduce the resistance of the continuous region 415. As a result, the sheet resistances of the source region 414 and t he continuous region 415 which are actually measured is 200 to 800 .OMEGA./.quadrature.. Then, as shown in FIG. 9D, a SiO.sub.2 film having a thickness of about 20 to 150 nm, about 100 nm in the present embodiment is formed as a gate insulating film 409 so as to cover the above-described island-like crystalline Si film. In the present embodiment, the SiO.sub.2 film is formed by using TEOS as a starting material, and decomposing and depositing it together with oxygen at a substrate temperature of about 300 to 400.degree. C. by an RF plasma CVD method. After the formation of the film, the gate insulating film 409 is annealed at about 400 to 600.degree. C. for several hours under an inert gas atmosphere in order to improve bulk property of the gate insulating film 409, and the interface property between the crystalline Si

film and the gate insulating film.

Detailed Description Paragraph Right (66):
Subsequently, an Al film having a thickness of about 300 to 600 nm, for example about 400 nm is formed by a sputtering method. Then, the Al film is patterned by any suitable method to form a gate electrode 410g and an upper electrode 410c of the storage capacitor Cs 434. In the active matrix substrate, the gate electrode 410g is formed from the n-th gate bus line, and the upper electrode 410c of the storage capacitor Cs is formed from the (n-th+1) gate bus line.

Detailed Description Paragraph Right (71):
Then, a liquid crystal display panel is fabricated using the active matrix substrate fabricated according to the present embodiment, and the overall display is performed. As a result, stripe-shaped uneven display that had appeared in the conventional liquid crystal display panel is not recognized and a liquid crystal display device having high display quality can be obtained.

Detailed Description Paragraph Right (72):
Still another preferred embodiment is illustrated with reference to FIG. 10, FIG. 11, FIGS. 12A to 12F, and FIGS. 13A to 13F. The present embodiment is a case where the present invention is applied to a driver monolithic-type active matrix substrate. In the present embodiment, the pixel TFT of the active matrix portion i s composed of an N-type TFT. Moreover, a TFT element which constitutes a driver circuit portion is formed on the same substrate as the pixel TFT is formed. The following illustrates a CMOS circuit which is composed complementarily of an N-type TFT and a P-type TFT as the TFTs for the driver circuit.

Detailed Description Paragraph Right (73):
FIG. 10 is a schematic plan view of the driver monolithic-type active matrix substrate; FIG. 11 is a schematic plan view for illustrating a method for fabricating a CMOS circuit constituting the driver circuit; FIGS. 12A to 12F are schematic sectional views for illustrating a method for fabricating the CMOS circuit, and sectional views taken along the XII--XII line of FIG. 10; and FIGS. 13A to 13F are schematic sectional views for illustrating a method for fabricating the pixel TFT.

Detailed Description Paragraph Right (74):
As shown in FIG. 10, the CMOS circuit of the driver monolithic-type active matrix substrate is composed of a plurality of N-type TFTs 522 and P-type TFTs 523 on the substrate, and its finished sectional structure is shown in FIG. 12F. FIG. 13F shows the finished sectional structure of the pixel TFT of the driver monolithic-type active matrix substrate. The following illustrates the structure of the semiconductor device as well as a method for fabricating it.

Detailed Description Paragraph Right (75):
First, as shown in FIGS. 12A and 13A, a base film 502 comprising SiO.sub.2 and having a thickness of approximately 300 nm is formed on a glass substrate 501 by, for example, a sputtering method. The SiO.sub.2 base film 502 is provided so as to prevent the impurities

contained in the glass substrate 501 from diffusing. Then, an intrinsic (I-type) amorphous Si (a-Si) film 503 having a thickness of about 20 to 100 nm, for example, about 50 nm is formed by a reduced pressure CVD method, a plasma CVD method, or the like.

Detailed Description Paragraph Right (76):
Then, a photosensitive resin (e.g., photoresist) is applied onto the a-Si film 503, and exposed to light and developed so as to form a photoresist mask 504. The a-Si film 503 is exposed in a slit shape in the region 500 by the throughhole of the photoresist mask 504 in the CMOS circuit portion. When the substrate of FIG. 12A is viewed from the top, the a-Si film 503 is exposed in a slit shape in the region 500 as shown in FIG. 11, and the other portions are masked by the photoresist. Furthermore, the photoresist mask 504 on the a-Si film 503 is all removed in the pixel TFT portion so that the entire surface of the a-Si film 503 is exposed, as shown in FIG. 13A.

Detailed Description Paragraph Right (77):
Then, as shown in FIGS. 12A and 13A, a catalyst element such as nickel is deposited on the thus-fabricated substrate 501 so as to form a catalyst element film 505. In the present embodiment, the thickness of the catalyst element (nickel) film 505 is adjusted to approximately 1 nm or less by making the distance between the deposition source and the substrate greater than usual to reduce the deposition rate. The surface density of the catalyst element (nickel) film 505 which is actually measured is approximately 1.times.10.sup.13 atoms/cm.sup.2. In a CMOS circuit as shown in FIG. 12A, the catalyst element (nickel) film on the mask 504 is lifted off by removing the photoresist mask 504. As a result, a slight amount of the catalyst element (such as nickel) is selectively added to the a-Si film 503 in the region 500. On the other h and, a slight amount of the catalyst element is added to the entire surface of the a-Si film 503 in a pixel TFT portion as shown in FIG. 13A. Then, the a-Si film is crystallized by annealing, for example, at a temperature of about 550.degree. C. for about 8 hours under an inert atmosphere.

Detailed Description Paragraph Right (78):
As shown in FIGS. 12B and 13B, this crystallization of the a-Si film 503 proceeds in the direction vertical to the substrate 501 using as a nucleus a catalyst element which has been added to the surface of the a-Si film 503, so as to form a crystalline Si-film 503b. In the CMOS circuit portion of FIG. 12B, the crystallization in the vertical direction only occurs in the region 500 to which a catalyst element is selectively added. Then, the crystal is grown in the horizontal direction (the direction parallel to the substrate) from the region 500 to a region surrounding the region 500 as indicated by the arrow 506 in FIGS. 11 and 12B, so as to form a horizontally grown crystalline Si film 503c. The other regions in the a-Si film 503 remain as an amorphous Si film region 503d. In the present embodiment, the size of the grown crystal in the direction parallel to the substrate is approximately 40 .mu.m.

Detailed Description Paragraph Right (79):
Thereafter, as shown in FIGS. 12C and 13C, a laser pulse 507 irradiates to recrystallize the Si film 503. The laser beams that

can be used include an XeCl excimer laser (having a wavelength of 308 nm and a pulse width of 40 nsec). The laser pulse 507 irradiates an energy density of about 200 to 350 mJ/cm.sup.2, for example about 320 mJ/cm.sup.2, while heating the substrate to about 200 to 500.degree. C., for example about 400.degree. C., at the time of the irradiation. The laser pulse 507 is shaped with a homogenizer so that the beam on the substrate surface has a slender rectangle shape (e.g., 150 mm.times.1 mm), and is successively scanned in the direction vertical to its longer side, i.e., the laser scanning direction 524 of FIG. 10. In the present embodiment, the overlapping amount of the beam in the successive scanning is set to be 95%. Therefore, the scanning pitch P in FIG. 10 is 50 .mu.m, and any one point of the a-Si film 503 is subjected to the laser irradiation twenty times each. According to this step, the crystalline Si film regions 503b and 503c are heated to a temperature higher than their melting points, and fused and solidified to be recrystallized films 508n and 508p which constitute an active region of the TFT of the CMOS circuit is designed to be 50 .mu.m, and the arrangement interval Xpg of the island-like crystalline Si film 508g which constitutes an active region of the pixel TFT is designed to be 100 .mu.m. That is, in the present embodiment, the arrangement interval Xpd of the TFT in the driver circuit (CMOS circuit) is designed to be the same as the laser scanning pitch P, and the arrangement interval Xpg of the pixel TFT is designed to be twice as much as the laser scanning pitch P. Since the layout of the driver circuit is independent of the arrangement interval of the pixel TFT, a driver circuit having higher integrity can be formed in any type of active matrix substrate. In FIG. 10, the symbols 521, 522 and 523 denote each TFT, and 527, 514 and 515 denote its channel region, source region and drain region, respectively.

Detailed Description Paragraph Right (81):
Thereafter, in the CMOS circuit portion, the prescribed portion of the crystalline Si film is removed by etching and patterned into a high quality and island-like crystalline Si film 503c' region which constitutes active TFT regions (element regions) 508n and 508p, as shown in FIGS. 11 and 12D. In the pixel TFT, as shown in FIG. 13D, the prescribed portion of the crystalline Si film is removed by etching and patterned into a high quality and island-like crystalline Si film 508g which constitutes an active region of the TFT. When the substrate 501 is viewed from the top, the island-like crystalline Si film 508g which constitutes an active region for each TFT is disposed as shown in FIG. 10. As can be seen from FIG. 10, in the present embodiment, the arrangement interval of the island-like crystalline Si film 508 (508n, 508p and 508g) in the laser light scanning direction 524 is different between the driver circuit portion and the pixel portion. Actually, the arrangement interval Xpd of the island-like crystalline Si TEOS as a starting material, and decomposing and depositing it together with oxygen at a substrate temperature of about 300 to 400.degree. C. by an RF plasma CVD method. Preferably, after the formation of the film, the gate insulating film 509 is annealed at about 400 to 600.degree. C. for several hours under an inert gas atmosphere in order to improve bulk property of the gate insulating film 509 as well as the interface property between the crystalline Si film and the gate insulating film 509.

Detailed Description Paragraph Right (83):
Then, impurities (e.g., phosphorus (P) and boron (B)) are doped into the island-like crystalline Si films 508n, 508p and 508g which constitute an active region by an ion doping method using the gate electrodes 510n, 510p and 510g as a mask. Phosphine (PH.sub.3) and diborane (B.sub.2 H.sub.6) are used as the doping gas. The accelerating voltage is about 60 to 90 kV, for example about 80 kV for P, and is about 40 to 80 kV, for example about 65 kV for B. The doping amount is about 1.times.10.sup.15 to 8.times.10.sup.15 cm.sup.-2, for example about 2.times.10.sup.15 cm.sup.-2 for P and is about 5.times.10.sup.15 cm.sup.-2 for B. According to this step, the regions 513n, 513p and 513g, which are masked by the gate electrodes 510n, 510p and 510g and into which no impurity is doped, constitute TFT channel regions 527n, 527p and 527g. In the doping operation, each impurity is selectively doped by covering the undesired region with a photoresist. As a result, an N-type impurity source region 514n and drain region 515n, and a P-type impurity source region 514p and drain region 515p are formed, so as to complete an N-channel type TFT 522 and a P-channel type TFT 523, as shown in FIGS. 12E and 12F. When the substrate is viewed from the top, as shown in FIG. 11, the crystal growth direction (as indicated by the arrow 506) in the island-like crystalline Si films 508n and 508p is parallel to the carrier moving direction (i.e., from the source to the drain direction). This arrangement provides a TFT having higher mobility.

Detailed Description Paragraph Right (88):
Then, a liquid crystal display panel is fabricated by using the driver monolithic-type active matrix substrate fabricated according to the present embodiment, and the overall display is performed. As a result, no stripe-shaped uneven display that appears to be caused by the successive laser scanning is recognized and a liquid crystal display device having high display quality can be obtained.

Detailed Description Paragraph Right (90):
Embodiments 1 and 2 illustrate only two cases where a relationship between a laser pulse scanning direction and a TFT channel direction is either parallel or vertical. These two cases are the simplest and the most easily understood, since a relationship between a TFT channel length X.sub.L and a laser scanning pitch P may be set when the scanning direction is parallel to the channel direction, and since a relationship between a TFT channel width X.sub.W and a laser scanning pitch P may be set when the scanning direction is vertical to the channel direction. However, the present invention is also applicable to, for example, a case where the laser pulse scanning direction is oblique to the TFT channel direction, which also provides excellent effects according to the present invention (i.e., much less unevenness of the crystallinity among the TFTs). In this case, the maximum length of the channel region of the TFT in the laser scanning direction may be set as a channel size defined by the present invention.

Detailed Description Paragraph Right (92):
Although Embodiments 2 and 5 employ a crystallization method using a catalyst element (i.e., an element accelerating the crystallization) in a solid phase crystal growth step, the same

effect can be attained by any suitable solid phase crystal growth method without using such a catalyst element. Moreover, the crystal is grown in the horizontal direction by selectively doping a catalyst element in Embodiment 2, but a crystal growth method may be used in which the catalyst element is not selectively doped, but doped into the entire surface of the Si film. In this case, an excellent effect is derived from the catalyst element, and also the method is simplified because of the lack of the necessity of a mask formation step.

Detailed Description Paragraph Right (94):
An active matrix-type substrate for a liquid crystal display device has been mainly illustrated as a preferred embodiment of the present invention, but the present invention is also applicable to, for example, adhesion-type image sensors, built-in driver-type thermal heads, built-in driver-type light writing devices and display devices having an organic EL element as an emission element, three-dimensional ICs, and thin film integrated circuits. According to the present invention, these devices having high performance (e.g., high speed, high resolution) can be obtained. The present invention is widely applicable to semiconductor processing (e.g., processing of bipolar transistors and electrostatic induction transistors using a crystalline semiconductor as an element material, in addition to the MOS-type transistors illustrated in the above-described embodiments).

Detailed Description Paragraph Right (96):
According to one aspect of the present invention, the semiconductor device includes a plurality of TFTs in which the channel region of the TFT comprises a crystalline Si film crystallized by the successive irradiation with a laser pulse in a scanning pitch P, and the size Xs of the channel region in the laser pulse scanning direction and the scanning pitch P of the laser pulse have a relationship approximately equal to Xs=nP (wherein n is an integer of 1 or more). Due to such a relationship between the size Xs of the channel region of the TFT and the scanning pitch P of the laser pulse, the channel region in each TFT contains all the possible crystallinity distributions in the scanning pitch P of the laser pulse along the laser pulse scanning direction. For example, with reference to the above-discussed FIG. 14B, every TFT channel region is crystallized to include the same crystallinity distribution (i.e., the difference in the crystallinity at the locations a to d). Therefore, although the channel region of each TFT has a crystallinity distribution, the crystallinity distribution is identical and thus each TFT has the same crystallinity. As a result, it is possible to eliminate the unevenness of the characteristics among the TFTs. Thus, the present invention is not intended to provide the uniformity of the characteristics among the TFTs by preparing a uniform crystalline Si film, but to accept the non-uniformity (crystallinity distribution) of the crystalline Si film obtained by the laser pulse scanning and then to accomplish the uniformity of the characteristics among the TFTs by utilizing its periodicity. When a liquid crystal display device is actually fabricated according to the present invention, and the characteristic uniformity of the pixel TFT is evaluated, excellent characteristic uniformity among the TFTs is obtained so as to prevent display defects resulted from the scanning of the laser

pulse. Therefore, according to the present invention, the remarkable improvement of the characteristic uniformity among a plurality of TFTs can provide a semiconductor device having high performance and excellent reliability as well as stability.

Detailed Description Paragraph Right (97):
The present invention is especially effective for applications requiring the characteristic uniformity of a plurality of TFTs. The typical example is an active matrix substrate for a liquid crystal display device. Since the quality (i.e., the uniformity of the TFT) of a liquid crystal display device is actually judged by the human eye, an extremely high uniformity in the element characteristics is required for the pixel TFT. The use of the present invention in the pixel TFT of a liquid crystal display device will significantly improve a uniformity among the TFTs. As a result, it is possible to prevent the display defects (for example, contrast unevenness) of a liquid crystal display device and thus to accomplish a liquid crystal display device having excellent display quality.

Detailed Description Paragraph Right (98):
In a driver monolithic-type active matrix semiconductor device having a pixel TFT arranged in a matrix shape and a driver circuit driving the pixel TFT on the same substrate, a plurality of the TFTs which constitute the driver circuit (especially, a shift resister circuit), as well as the pixel TFT, require an extremely high characteristic uniformity. This is because the unevenness in the TFT characteristic of the driver circuit provides a different driving wave in each line, which results in the formation of a stripe-shaped uneven display on the screen. Since human eyes are very accurate and have a capability of distinguishing even a slightly uneven display, an excellent characteristic uniformity is required for the TFT so as to reduce the uneven display to the level that the uneven display is not recognized by human eyes. When the present invention is applied to a driver monolithic-type active matrix semiconductor device, the channel regions of the TFTs which constitute the driver circuit have a crystallinity distribution that results from the laser pulse scanning, but the channel region of each TFT has the same crystallinity. Therefore, excellent characteristic uniformity in the overall TFTs can be obtained. As a result, the characteristics of the driver circuit driving the pixel TFT will be stabilized so as to reduce defects such as uneven display that result from the unevenness of the characteristics in the driver circuit of the liquid crystal display device. Moreover, since a driver monolithic-type active matrix semiconductor device having high performance, high integrated and characteristically uniform TFTs which constitute the driver circuit can readily be obtained at a lower cost, it is possible to provide a compact, high performance and less expensive module.

Detailed Description Paragraph Right (99):
In a preferred embodiment, the size Xs of the TFT channel region in the laser pulse scanning direction and the scanning pitch P of the laser pulse are approximately the same, i.e., have a relationship approximately equal to Xs=P. This is because it is necessary to irradiate the substrate in the maximum pitch in view of throughput, since the irradiation number of the laser pulse is increased as the area of the substrate is increased. In the case where the size Xs